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EXAMINER	
CAMPOS, YAIMA	
ART UNIT	**PAPER NUMBER**
2185	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/656,639	DURRANT, PAUL	
	Examiner	Art Unit	
	Yaima Campos	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/12/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The instant application having Application No. 10/656,639 has a total of 30 claims pending in the application; there are 3 independent claims and 27 dependent claims, all of which are ready for examination by the examiner.

I. INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

2. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in **37 C.F.R. 1.63.**

II. STATUS OF CLAIM FOR PRIORITY IN THE APPLICATION

As required bye **M.P.E.P. 201.14(c)**, acknowledgement is made of applicant's claim for priority based on an application filed on September 6, 2002 (Foreign Priority 02256209.4). It is noted, however, that applicant has not filed a certified copy of the application as required by **35 U.S.C. 119(b)** and **M.P.E.P. 201.14(b)**.

III. INFORMATION CONCERNING DRAWINGS

Drawings

3. The applicant's drawings submitted are acceptable for examination purposes.

IV. ACKNOWLEDGEMENT OF REFERENCES CITED BY APPLICANT

4. As required by **M.P.E.P. 609(C)**, the applicant's submissions of the Information Disclosure Statement dated April 12, 2004 is acknowledged by the examiner and the cited references have been considered in the examination of the claims now pending. As required by **M.P.E.P 609 C(2)**, a copy of the PTOL-1449 initialed and dated by the examiner is attached to the instant office action.

V. REJECTIONS NOT BASED ON PRIOR ART

a. DEFICIENCIES IN THE CLAIMED SUBJECT MATTER

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. **Claims 2-8 and 10-13** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. As per **claim 2**, claim 2 recites the limitation "a memory controller" in line 2. As best understood by the examiner, this limitation refers to the same "controller" as specified in claim 1; however, it is unclear whether the applicant refers to one controller or to different controllers. Therefore, claim 2 is considered as being vague, indefinite and lacking antecedent basis. The applicant might consider amending this claim to read **--the controller--.**

8. As per **Claim 4**, claim 4 recites the limitations "said controller" and "said memory controller" in lines 1 and 2. The examiner interprets that both of these

limitations refer to the "controller" of claim 1; however, it is unclear whether the applicant refers to one controller or to different controllers. Therefore, claim 4 is considered as being vague, indefinite, and lacking antecedent basis. The applicant might consider amending this claim to read – **the controller --.**

Claim 4 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Claim 4 appears to replicate the contents of claim 2; the claim on which it depends.

Appropriate correction is required.

9. As per **Claim 5**, lines 2 and 4 recite "a first memory controller" and "a second memory controller." The examiner interprets that both of these limitations refer to the "controller" of claim 1. Therefore, claim 4 is considered as being vague, indefinite, and lacking antecedent basis. The applicant might consider amending this claim by adding – **wherein the controller comprises a first memory controller and a second memory controller --.**

10. As per **claim 8**, claim 8 recites the limitations "said controller" and "said first and second memory controllers" in lines 1 and 2. As best understood by the examiner, it appears that the "first and second memory controllers" refer to the "controller" of claim 1. Therefore, claim 4 is considered as being vague, indefinite, and lacking antecedent basis. The applicant might consider amending

this claim by adding – **wherein, the controller comprises a first memory controller and a second memory controller --.**

Claim 8 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Claim 4 appears to replicate the contents of claim 5; the claim on which it depends.

Appropriate correction is required.

11. As per **claim 10**, claim 10 recites the limitation "the processor is allowed to continue processing." A reference does not prohibit a computer from doing the recited acts. It is unclear what Applicant's intended metes and bounds of the claim are, since the claim appears to cover anything and everything that does not prohibit actions from occurring. The applicant might consider amending this claim to read – **the processor continues processing --.**

12. Any claim not specifically addressed above, is being rejected as encompassing the deficiencies of a claim upon which it depends.

VI. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 102

13. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

14. **Claims 1-4, 9-10, 17-25** are rejected under 35 U.S.C. 102(e) as being anticipated by Garret et al. (US 6,408,369).

15. As per **claims 1 and 22**, Garret discloses "a computer system including a processor" **[Garret discloses that "the system further comprises a control processor" (Column 1, lines 48-49) and "Hosts 12a-12n" (Figure 1)]**

"a controller" **["Memory controller 14" (Figure 1)]**

"a data communications facility interconnecting said processor and controller" **["Busses 36" (Figure 1)]**

"a memory having a plurality of locations for storing data" **["Disk drives 16a-16k" and "Tape storage devices 18a-18k" (Figure 1)]**

"wherein said controller is responsive to a single command received from the processor to copy data from a first memory location to a second memory location, wherein said single command specifies said first and second memory locations" **[With respect to this limitation, Garret discloses a system and method featuring the "transfer of data from a first storage device to a second storage device" (Column 1, lines 34-35) where "the controller receives a transfer command from the outside source" (Column 1, lines 48-50) which is specified to be a processor (Column 1, lines 38-39). It is**

inherent that a command that's moving data from one memory location to another must have both, the source and destination locations included in the command. (Reference cited for inherency in section VII)].

16. As per **claim 2**, Garret discloses "a computer system" **[See rejection to claim 1]** "wherein said memory is coupled to said data communications facility via a memory controller" **[With respect to this limitation, Garret discloses Busses connecting "memory controller 14" to "tapes 18a-18k" and busses connecting "memory controller 14" to "disk drives 16a-a6k" (Figure 1)].**

17. As per **claims 3 and 24**, Garret discloses "a computer system" **[See rejection to claim 1]** "wherein the data is copied from the first memory location to the second memory location by an internal memory transfer" **[Garret discloses this limitation as it is taught that "the transfer is made internally of the storage controller rather than requiring the command processors to communicate directly with each other" (Columns 1-2, lines 65-67 and 1)]** "without traveling over the data communications facility" **[With respect to this limitation, Garret discloses that "the busses connecting the host computer to the disk drive controller are also not used and remain free for other operations" (Column 3, lines 48-50)].**

18. As per **claim 4**, Garret discloses "a computer system" **[See rejection to claim 1]** "wherein said controller is provided by said memory controller" **["Memory controller 14" (Figure 1)].**

19. As per **claim 9,** Garret discloses "a computer system" **[See rejection to claim 1]** "wherein the controller maintains a record of copy operations that are

currently in progress" **[With respect to this limitation, Garret discloses that a controller sets "a state of the pending stored data as a write pending state" and later "destages the write pending memory stored data to the second storage device" (Column 1, lines 40-45) as a way for the controller of keeping a record and control of the operations currently being processed].**

20. As per **claims 10 and 25**, Garret discloses "a computer system" **[See rejection to claim 1]** "wherein the processor is allowed to continue processing operations prior to completion of the copy" **[Garret discloses "a command processor host computer with the additional selected ability to transfer data without itself being involved in the physical transfer process" (Column 2, lines 6-9) because "controller 14" is in charge of the transfer of data (Column 1, lines 53-54)].**

21. As per **claim 17**, Garret discloses "a computer system" **[See rejection to claim 1 above]** "wherein said processor supports a specific programming command to copy data from a first memory location to a second memory location" **[With respect to this limitation, Garret discloses a method that "features receiving an internal copy command from a commanding processor over a controller" (Column 1, lines 38-39); this command comprising a "transfer of physical data from a first storage device to a second storage device" (Column 1, lines 33-35)].**

22. As per **claim 18**, Garret discloses "a computer system" **[See rejection to claim 1]** "wherein said data communications facility is a bus" **["Busses 36," "busses" connecting "memory controller 14" to "tapes 18a-18k" and**

"busses" connecting "memory controller 14" to "disk drives 16a-16k" (Figure 1)].

23. As per **claims 19 and 23**, Garret discloses "a computer system" **[See rejection to claim 1]** "wherein said bus supports a command set, and said single command is part of said command set" **[With respect to this limitation, Garret discloses that "the host computer sends a system command over a channel, the SCSI channel or the fiber channel" (Column 3, lines 51-54)].**

24. As per **claim 20**, Garret discloses "a computer system" **[See rejection to claim 1]** "wherein said controller transmits an acknowledgement of said single command back to the processor, and wherein the processor is responsive to a failure to receive said acknowledgement within a predetermined time-out period to perform said copy operation by issuing separate read and write commands" **[With respect to this limitation, Garret discloses that "the controller returns a *command not completed* back to the host computer and the host computer can either try the operation again, or transfer the data using a *prior art* command sequence" (Columns 3-4, lines 66-67 and 1-3) where the "*prior art* command sequence" involves "reading data from one disk drive unit into its own memory and then writing the data from its own memory to a second disk drive unit" (Column 1, lines 14-16)].**

As per **claim 21**, this claim requires "data communications means for interconnecting said processor means and said controller means" ***(page 12, line 6 and figure 1 of applicant's specification defines the means as a bus)***. **[Garret teaches this limitation as "Busses 36" (Figure 1)]** "memory means

having a plurality of locations for storing data" (***page 14, line 10 and figure 1 of applicant's specification defines the means as RAM 40)***. **[With respect to this limitation, Garret teaches "Global memory 32" (Figure 2)]** "wherein said controller means includes means responsive to a single command received from the processor means for copying data from a first memory location to a second memory location, wherein said single command specifies said first and second memory locations" (***page 5 and figure 1 of applicant's specifications defines the means for copying as Memory Controller 35***). **[Garret teaches a "Memory Controller 14" that meets this limitation].**

Claim Rejections - 35 USC § 103

25. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

26. **Claims 5-8** are rejected under 35 U.S.C. 103(a) as being unpatentable over Garret et al. (US 6,408,369) in view of Busser et al. (US 6,732,243).

27. As per **claims 5 and 8**, Garret discloses "a computer system" as disclosed in claim 1 **[See rejection to claim 1 above]** but does not disclose expressly that "a first portion of memory is coupled to said data communications facility via a first memory controller and includes said first memory location, and a second

portion of memory is coupled to said data communications facility via a second memory controller and includes said second memory location."

Busser discloses a system and method where "a first portion of memory is coupled to said data communications facility via a first memory controller and includes said first memory location, and a second portion of memory is coupled to said data communications facility via a second memory controller and includes said second memory location". Busser teaches a **[method and apparatus for mirroring data in a storage system (Column 4, lines 44-45)]** including **["a first controller management module" (Column 4, lines 45-46) and "a second controller management module" (Column 4, lines 51-52) wherein the "first controller memory module" has "a first memory" (Column 13, lines 63-67) and the "second controller memory module" has "a second memory" (Column 14, lines 1-3)]**. Busser also teaches that **["data is mirrored from the first controller management module to the second controller management module" (Column 4, lines 48-61)]** and that **[the controllers are connected to a bus (Column 2, line 12)]**.

Garret et al. (US 6,408,369) and Busser et al. (US 6,732,243) are analogous art because they are from the same field of endeavor of copying/transferring data from one memory location to another.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to make the system for transferring data from one memory location to another include two different controllers, one controlling a first memory

location and the other controlling a second memory location, as described by Busser.

The motivation for doing so, as taught by Busser, would have been that by having two different "controller management modules" controlling each of two different memory locations, **["data is mirrored from the first controller management module to the second controller management module using the first direct memory access engine while avoiding interruption to the second processor" (Column 4, lines 58-61) and vice versa]**. Busser also teaches that this approach is useful because it **["reduces the processing overhead involved with mirroring data" (Column 4, lines 38-39)]**.

Therefore, it would have been obvious to combine Busser et al. (US 6,732,243) and Garret et al. (US 6,408,369) for the benefit of creating a system and method for transferring data from one memory location to another to obtain the invention as specified in claims 5 and 8.

As per **claims 6 and 7**, Busser discloses "a computer system" **[See rejections to claims 1 and 5 above]** "wherein the data is copied from the first memory location to the second memory location by using a peer-to-peer copy operation on the data communication facility" and "wherein said data communications facility supports direct memory access (DMA), and said peer-to-peer copy operation is performed by using a transaction analogous to DMA." Busser teaches a system to transfer data from one memory location to another that uses **["DMA mirroring;" he also explains that "DMA is a capability provided by some computer bus architectures" (Column 10, lines 18-28)]**.

Busser further explains that having a "data mirroring system" that uses "DMA transfer" allows for faster processing because **[it does not consume the computer's processing resources (Column 10, lines 25-28)]**.

28. **Claims 11-12 and 26-27** are rejected under 35 U.S.C. 103(a) as being unpatentable over Garret et al. (US 6,408,369) in view of O'Brien et al. (US 6,038,639).

29. As per **claims 11 and 26**, Garret discloses a computer system according to claim 10 **[See rejections to claim 10 above]** but does not disclose expressly that "the controller redirects a read request for the second memory location to the first memory location if the copy has not yet completed."

O'Brien discloses a system for transferring data from one memory location to another wherein "the controller redirects a read request for the second memory location to the first memory location if the copy has not yet completed." O'Brien teaches this limitation as it is explained that **["a request to read data from the copy data file received before the mapping table pointers have been updated is redirected to the original data file" (Column 4, lines 40-43)]**.

Garret et al. (US 6,408,369) and O'Brien et al. (US 6,038,639) are analogous art because they are form the same field of endeavor of copying/transferring data from one memory location to another.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to make the system for transferring data from one memory location to another as described by Garret further provide a method so that once a copy command is issued by a processor; any read command to the destination

location is redirected to the source location as long as the copy operation has not been completed, as taught by O'Brien.

The motivation for doing so would have been because O'Brien teaches that any read command to the destination location is redirected to the source location as long as the copy operation has not been completed **["to ensure that the data file read operation behaves as though the snapshot copy process had been completed" (Column 4, lines 40-44) in order to guarantee "copy data file correspondence to the original data file" (Column 4, lines 49-50)]**.

Therefore, it would have been obvious to combine O'Brien et al. (US 6,038,639) with Garret et al. (US 6,408,369) for the benefit of creating a system and method to copy/transfer data from one memory location to another as specified in claims 11 and 26.

30. As per **claims 12 and 27**, O'Brien teaches a system as specified in claim 10 **[See rejection to claim 10 above]**, "wherein the controller delays a write request for the first memory location pending completion of the copy" as it is taught that **["Any attempt to update the mapping table to reflect data written to the original data file of the copy data file that occurs after initiation of the snapshot copy operation must wait until the first set of mapping table pointers have been updated" (Column 3, lines 26-30)]**.

31. **Claim 13 and 28** are rejected under 35 U.S.C. 103(a) as being unpatentable over Garret et al. (US 6,408,369) in view of Kinjo et al. (US 5,701,437).

32. As per **claims 13 and 28**, Garret discloses a computer system according to claim 10 **[See rejections to claim 10 above]** but does not disclose expressly that "in response to a write request for the second memory location prior to completion of the copy, the controller cancels completion of the copy for the part of the second memory location subject to the write request."

Kinjo discloses a system for transferring data from one memory location to another "wherein in response to a write request for the second memory location prior to completion of the copy, the controller cancels completion of the copy for the part of the second memory location subject to the write request." Kinjo discloses a system for transferring data from one location to another that includes **["canceling the memory copy operation upon completion of the write access to the memories when a write instruction is transmitted form one of the plurality of processors to the plurality of memories before the memory copy operation is performed" (Columns 4 and 5, lines 65-67 and 1-3)]**.

Garret et al. (US 6,408,369) and Kinjo et al. (US 5,701,437) are analogous art because they are form the same field of endeavor of copying/transferring data from one memory location to another.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to make the system for transferring data from one memory location to another as described by Garret further provide a method so that once a copy command is issued, any write command to the destination location results

in the copy command being cancelled as long as the copy operation has not been completed, as taught by Kinjo.

The motivation for doing so would have been because Kinjo teaches that any write command to the destination location results in the copy command being cancelled as long as the copy operation has not been completed so that a **["copy operation can be performed without complicating a hardware mechanism and lowering capacity of the apparatus (Column 3, lines 24-26). Kinjo also teaches that this method improves copy efficiency (Column 3, line 30)]**.

Therefore, it would have been obvious to combine Kinjo et al. (US 5,701,437) with Garret et al. (US 6,408,369) for the benefit of creating a system and method to copy/transfer data from one memory location to another as specified in claims 13 and 28.

33. **Claims 14-16 and 29-30** are rejected under 35 U.S.C. 103(a) as being unpatentable over Garret et al. (US 6,408,369) in view of Bailey (US 5,802,559).

34. As per **claims 14 –15 and 29**, Garret discloses "a computer system" **[See rejection to claim 1 above]** "further comprising a cache" **[With respect to this limitation, Garret teaches that "The storage system, according to the invention, features a storage controller having a cache memory" (Column 1, lines 46-47)]**.

Garret does not disclose expressly that "any cache entry for the second memory location is invalidated in response to said single command" by a processor.

Bailey discloses a system and method for updating the data stored in cache memory where "any cache entry for the second memory location is invalidated in response to said single command" by a processor. Bailey discloses that **["when an alternate bus master attempts to write data to system memory" and "a corresponding cache line is contained within the cache memory" and "the line is clean, the line is marked invalid by the cache controller and the transfer of data from the alternate bus master into system memory is allowed to complete" (Column 2, lines 53-65)]**.

Garret et al. (US 6,408,369) and Bailey (US 5,802,559) are analogous art because they are from the same field of endeavor of copying/transferring data from one memory location to another.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to make the system for transferring data from one memory location to another including a cache as described by Garret, further provide a method so that once a copy command is issued by a processor; any cache entries pertaining to the destination location are invalidated, as taught by Bailey.

The motivation for doing so would have been because Bailey teaches that once a copy command is issued by a processor, any cache entries pertaining to the destination location are invalidated as a way of preventing **["an incoherence between the cache memory and system memory" (Column 2, lines 29-32)]**.

Therefore, it would have been obvious to combine (US 6,408,369) by Garret et al. with (US 5,802,559) by Bailey for the benefit of creating a cache flushing system to obtain the invention as specified in claims 14-15 and 29.

35. As per **claims 16 and 30**, Bailey discloses a system and method for updating the data stored in cache memory "wherein any updated cache entry for the first memory location is flushed to memory in response" to a memory transfer. Bailey specifically teaches that **[if a line of data in cache is dirty, the cache controller then causes the entire line of dirty data within the cache memory to be written back into system memory by "executing a burst write cycle to system memory" (Column 3, lines 2-9) as a way of maintaining coherency between the data in cache and the data in memory]**.

VII. RELEVANT ART CITED BY THE EXAMINER

36. The following prior art made of record and not relied upon is cited to establish the level of skill in the applicant's art and those arts considered reasonably pertinent to applicant's disclosure. See **MPEP 707.05(c)**.

37. The following reference teaches a computer system comprising a single memory copy command "wherein said single command specifies said first and second memory locations."

U.S. PATENT NUMBER

US 6,516,343

VIII. CLOSING COMMENTS

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

38. The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

a(1) CLAIMS REJECTED IN THE APPLICATION

39. Per the instant office action, claims 1-30 have received a first action on the merits and are subject of a first action non-final.

b. DIRECTION OF FUTURE CORRESPONDENCES

40. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yaima Campos whose telephone number is (571) 272-1232. The examiner can normally be reached on Monday to Friday 8:00 AM to 4:30 PM.

IMPORTANT NOTE

41. If attempts to reach the above noted Examiner by telephone are unsuccessful, the Examiner's supervisor, Mr. Donald Sparks, can be reached at the following telephone number: Area Code (571) 272-4201.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on

access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

November 1, 2005

Yaima Campos
Examiner
Art Unit 2185

DONALD SPARKS
SUPERVISORY PATENT EXAMINER